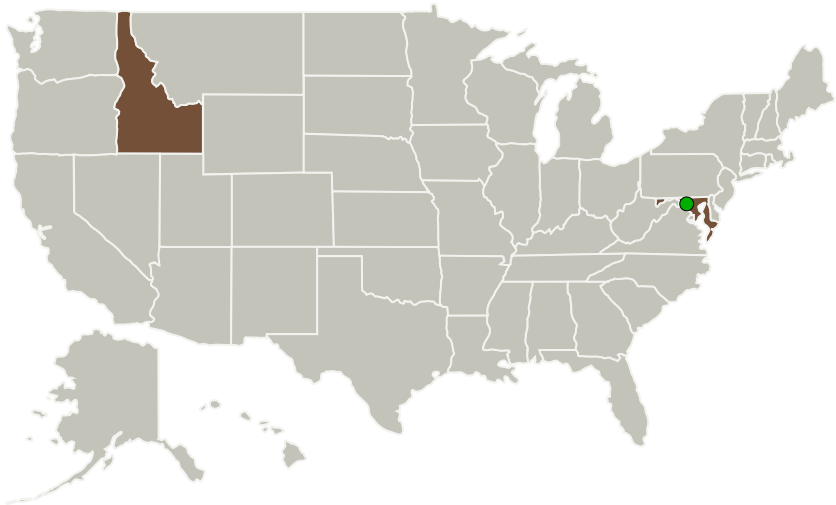
A 45 nm Low Cost, Radiation Hardened, Platform Based Structured ASIC, Phase I

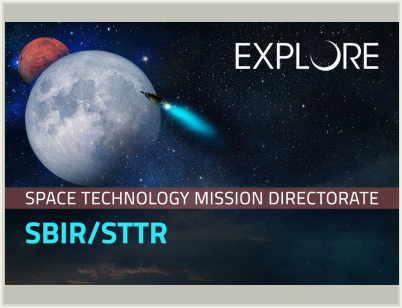
Completed Technology Project (2012 - 2012)

Project Introduction

The proposed 45 nm radiation hardened platform based structured ASIC architecture offers the performance and density expected of a custom ASIC with the low manufacturing cost associated with a structured ASIC. The low cost, high performance customization of the structured ASIC portion of the chip is made possible by the 1-D 45 nm Mask-Lite process technology. The chip architecture is optimized for sensor data handling applications in space and the design process provides for a short development schedule. The architecture provides a hard macro microcontroller core with via-ROM program memory, SRAM data memory, CPU support logic, an appropriate set of analog functions, and a structured ASIC section for application specific functionality. A rad-hard by design logic cell library is provided for the structured ASIC area of the die along with a number of pre-compiled macro functions such as timers and serial I/O to reduce development time. The 1-D Mask-Lite process provides a dramatic reduction in the mask cost, allowing lower volume designs to gain access to 45 nm technology, and provides performance improvement over conventional via mask structured ASIC technologies by eliminating metal layer stubs. Standard logic design, verification and layout EDA tools are used to complete a chip design. The fixed microcontroller platform portion of the chip is implemented with optimized standard cells rather than the structured ASIC logic cells, resulting in standard ASIC performance levels for the core logic.

Primary U.S. Work Locations and Key Partners





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Small Business Innovation Research/Small Business Tech Transfer

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Organizations Performing Work	Role	Type	Location
American Semiconductor, Inc.	Lead Organization	Industry	Boise, Idaho
Goddard Space Flight Center(GSFC)	Supporting Organization	NASA Center	Greenbelt, Maryland

Primary U.S. Work Locations	
Idaho	Maryland

Project Transitions

February 2012: Project Start

August 2012: Closed out

Closeout Documentation:

- Final Summary Chart*(https://techport.nasa.gov/file/137804)*

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

American Semiconductor, Inc.

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

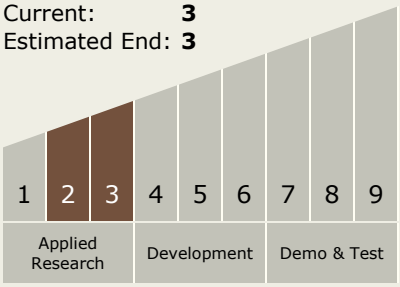
Carlos Torrez

Principal Investigator:

William Tiffany

Technology Maturity (TRL)

Start: **2**
Current: **3**
Estimated End: **3**



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Completed Technology Project (2012 - 2012)

Technology Areas

Primary:

- TX02 Flight Computing and Avionics
  - TX02.1 Avionics Component Technologies
    - TX02.1.6 Radiation Hardened ASIC Technologies

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System